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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,714	10/12/2001	Timothy J. Maloney	42390P11991	2480

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,714	MALONEY ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/04/03 have been fully considered but they are not persuasive.

Applicant argues that Maloney et al fails to disclose the limitation that the second current sink transistor has a current carrying electrode to receive a ground voltage potential. The examiner points to transistor (406) as being the second transistor; and as shown in figure 4 it is connected to ground (see rejection below for further explanation).

Applicant argues that Maloney et al fails to disclose a second tier that includes a second current sink transistor. Applicant argues that figure 5 of Maloney et al. shows that the first and second tier are connected lo the same current sink transistor. The examiner points to figure 4 showing first tier (426, 443, 442, 424, 416) and a first current sink transistor (406); and second tier (418, 422, 420, 441, 440) and second current sink (402/404) as claimed by the amended claim 9. Therefore, for the reasons above the examiner maintains the rejections.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 6, 9-14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Maloney (US 5,956,219).

As to claims 1 and 2, Maloney figure 4 discloses a voltage divider (410, 412) to provide a first intermediate voltage potential (416); a first current sink transistor (404); a second current sink transistor (406) in series with the first and having a current carrying electrode to receive a ground voltage potential (gnd); and a first drive circuit (428, 426, 424) to provide an enabling voltage potential to the second current sink (406); wherein the drive circuit comprises an inverter (426) with an input (443) coupled to receive the first intermediate voltage potential (416).

As to claims 3, the first current sink transistor and the second current sink transistor are formed in a same well in a semiconductor substrate (col. 3 lines 48-50).

As to claim 5, the ESD device further comprises: a third current sink transistor (402) coupled in series with the first current sink transistor (404); and a second drive (422, 420, 418) circuit to provide an enabling voltage potential to the third current sink transistor.

As to claim 6, the voltage divider (408, 410, 412) is adapted to provide a second intermediate voltage potential (414) and the second drive circuit comprises an inverter (420) with an input (441) coupled to receive the second intermediate voltage potential (414).

As to claim 9, static random access memory (col. 3 line 33); and an integrated circuit (figure 1, 100), the integrated circuit having an electrostatic protection circuit (figure 4) comprising: first tier (426, 443, 442, 424, 416) and including an RC timer (424) and a first current sink transistor (406); and second tier (418, 422, 420, 441, 440) wherein the second tier is coupled to the RC timer (424 through 414, 410, 416 or through 420) and second current sink (402/404).

As to claim 10, further comprising a voltage divider (408, 410, 412) coupled to the first tier and the second tier to provide an intermediate voltage potential (414).

As to claim 11, wherein the second tier includes an inverter (420) having an input terminal (thru 441) coupled to receive the intermediate voltage potential (414).

As to claims 12 and 13, the first tier includes an inverter (426) having an input terminal coupled to the RC timer (424 through 443, 416, 410, 414 or through 442, 420); transistor and capacitor (442, 443).

As to claim 14, [renumber the elements of claims 9, 12, and 13 as follows: first tier (418, 422, 420, 441, 440) and including an RC timer (418) and a first current sink transistor (402/404); and second tier (426, 443, 442, 424, 416) wherein the second tier is coupled to the RC timer (418 through 414, 410, 416 or through 420) and second current sink (406), the first tier includes an inverter (420) having an input terminal coupled to the RC timer (418); transistor and capacitor (440, 441)], capacitor (441) and intermediate voltage potential (414).

As to claim 17, the voltage divider (408, 4101, 412) comprises at least two transistors coupled in series between voltage potential rails (Vcc and ground) (figure 4).

4. Claims 4, 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maloney (US 5,956,219).

As to claim 4 Maloney discloses the claimed invention as stated above in regards to claim 1 except for wherein the first current sink transistor and the second current sink transistor are formed in different wells in a semiconductor substrate. Forming transistors on different wells in a semiconductor substrate is known in the art and would not add novelty to the claimed invention.

Therefore, the examiner take official notice that it would have been oblivious to one having ordinary skill in the art at the time the invention was made to form the first current sink transistor and the second current sink transistor in different wells in a semiconductor substrate in order to provide both p-type and n-type transistors.

As to claim 7, Maloney discloses the claimed invention as stated above in regards to claim 1 except for wherein the voltage divider comprises at least four transistors coupled in series.

Maloney does disclose, in figure 3, coupling two transistors in series (302, 304) to form a voltage divider. And then in figure 3 Maloney discloses coupling three transistors in series (408, 410, 412) to form a voltage divider with an additional tap in order to provide a second intermediate voltage potential to be used by the circuit.

Therefore, to add a fourth transistor in series with the other three is considered to be merely determining an optimum value and it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a fourth transistor in series with the existing three in order to tap a third potential voltage to be used in the circuit or to add additional voltage divider elements to divide the input voltage to a desired or proper voltage for circuit use since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 167 F.2d 272, 205 USPQ 215 (CCPA 1980).

As to claim 15, Maloney discloses the claimed invention as stated above in regards to claim 9 except for wherein the voltage divider comprises at least four transistors coupled in series.

Maloney does disclose, in figure 3, coupling two transistors in series (302, 304) to form a voltage divider. And then in figure 3 Maloney discloses coupling three transistors in series (408, 410, 412) to form a voltage divider with an additional tap in order to provide a second intermediate voltage potential to be used by the circuit.

Therefore, to add a fourth transistor in series with the other three is considered to be merely determining an optimum value and it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a fourth transistor in series with the existing three in order to tap a third potential voltage to be used in the circuit or to add additional voltage divider elements to divide the input voltage to a desired or proper voltage for circuit use since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 167 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maloney (US 5,956,219).

As to claim 8, Maloney discloses the claimed invention as stated above in regards to claim 1 except for wherein the ESD device further comprises a latch coupled to the voltage divider; and s to claim 16. Maloney discloses the claimed invention as stated above in regards to claim 9 except for further comprising a latch coupled to the voltage divider.

Pilling et al teaches coupling a latch circuit (118) to a voltage divider (Q2, Q3, Q7) in a circuit for improving the reliability of antifuses by storing the state of an antifuse in a latch and thus is available for continuous sampling without subjecting the antifuse to additional read voltages, since an antifuse coupled to a programming pin and all other antifuses are susceptible

to damage from ESD levels unless they are adequately protected from the ESD levels (col. 2 and col.3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Maloney to add a latch to the voltage divider as taught by Pilling et al in order to couple the latch circuit to a voltage divider to store the state of any particular part of the circuit to be available for sampling at a desired time in order to determine the state of the circuit after sampling.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/8/04

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